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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,745	10/06/2003	Mitchell Alsup	5500-89200	2802
53806	7590	02/06/2006		
MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL (AMD)			EXAMINER	
P.O. BOX 398			CODY, DILLON J	
AUSTIN, TX 78767-0398			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/679,745		ALSUP ET AL.	
	Examiner		Art Unit	
	Dillon Cody		2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) ☐ Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>16 September 2004</u> . | 6) ☐ Other: _____ |

DETAILED ACTION

1. Claims 1-23 are pending.

Papers Filed

2. Examiner acknowledges receipt of claims, disclosure, drawings, and declaration, all filed 6 October 2003; information disclosure statement filed 16 September 2004.

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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6. Claims 1-4, 6-9, 12-15, 17-20 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson (U.S. Patent No. 5,129,067).

7. As per claim 1, Johnson discloses a microprocessor comprising:

a plurality of functional units (Fig. 6 functional units 22-30), wherein said plurality of functional units is configured to collectively operate on a maximum number of operands in a given execution cycle; (Col. 4 lines 61-62)

a register file (Fig. 6 register file 18) providing a number of read ports that is insufficient to provide said maximum number of operands to said plurality of functional units in said given execution cycle; (Col. 4 lines 57-58)

and an arbitration logic (Fig. 9 decode arbitration 52) coupled to allocate said read ports of said register file for use by selected functional units during said given execution cycle. (Col. 4 lines 53-64)

8. As per claim 2, Johnson discloses the microprocessor as recited in claim 1, wherein each of said plurality of functional units corresponds to one of a plurality of issue slots. *The examiner asserts that any instruction issued from the decoder to a given functional unit fulfills an issue slot for that unit.*

9. As per claim 3, Johnson discloses the microprocessor as recited in claim 2, wherein said arbitration logic is further configured to allocate a first portion of said read ports to a first portion of said plurality of functional units that corresponds to a first issue

slot. *The examiner asserts that a given read port can be assigned to any functional unit, as pictured in Fig. 6.*

10. As per claim 4, Johnson discloses the microprocessor as recited in claim 3, wherein said arbitration logic is further configured to allocate a second portion of said read ports to a second portion of said plurality of functional units that corresponds to a second issue slot. *The examiner asserts that a given read port can be assigned to any functional unit, as pictured in Fig. 6. Further, multiple functional units operate on multiple instructions at the same time, as evidenced by the term "super-scalar". (Col. 4 lines 3-4)*

11. As per claim 6, Johnson discloses the microprocessor as recited in claim 1 wherein each of said plurality of functional units corresponds to one of a plurality of functional unit types. *The examiner asserts that all functional units have a type (i.e., ALU 24 is of the ALU type, shifter 26 is of the shifting type).*

12. As per claim 7, Johnson discloses the microprocessor as recited in claim 6, wherein said arbitration logic is further configured to allocate a first portion of said read ports to a first portion of said plurality of functional units that corresponds to a first functional unit type. *The examiner asserts that the read ports can be assigned to any instruction, no matter what function the instruction performs. The port(s) assigned to an*

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instruction (which will run on a functional unit which has a functional unit type) constitute the first portion of ports.

13. As per claim 8, Johnson discloses the microprocessor as recited in claim 7, wherein said arbitration logic is further configured to allocate a second portion of said read ports to a second portion of said plurality of functional units that corresponds to a second functional unit type. *The examiner asserts that the port(s) assigned to a second instruction (which will run on a second functional unit which has a functional unit type) constitute the second portion of ports.*

14. As per claim 9, Johnson discloses the microprocessor as recited in claim 1 further comprising a scheduler configured to assign one of a plurality of operations to a respective one of said plurality of functional units and to store an age of each of said plurality of operations, wherein said arbitration logic is further configured to allocate a first portion of said read ports to a given respective functional unit dependent upon said age of a corresponding operation. *The examiner asserts that if an instruction is not issued to the functional units in the cycle it was fetched and decoded, it will be held until a subsequent cycle. Col. 4 line 64 – col. 5 line 5 discloses the situations if one to four prior instructions are pending: some of the new instructions do not issue. The decode/issue logic must inherently keep track of which instructions have been held over from a prior cycle if this is to be the case.*

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15. As per claim 12, Johnson has taught a method performing the same function as the processor of claim 1, consequently claim 12 is rejected for the same reasons set forth in the rejection of claim 1 above.

16. As per claim 13, Johnson has taught a method performing the same function as the processor of claim 2, consequently claim 13 is rejected for the same reasons set forth in the rejection of claim 2 above.

17. As per claim 14, Johnson has taught a method performing the same function as the processor of claim 3, consequently claim 14 is rejected for the same reasons set forth in the rejection of claim 3 above.

18. As per claim 15, Johnson has taught a method performing the same function as the processor of claim 4, consequently claim 15 is rejected for the same reasons set forth in the rejection of claim 4 above.

19. As per claim 17, Johnson has taught a method performing the same function as the processor of claim 6, consequently claim 17 is rejected for the same reasons set forth in the rejection of claim 6 above.

20. As per claim 18, Johnson has taught a method performing the same function as the processor of claim 7, consequently claim 18 is rejected for the same reasons set forth in the rejection of claim 7 above.

21. As per claim 19, Johnson has taught a method performing the same function as the processor of claim 8, consequently claim 19 is rejected for the same reasons set forth in the rejection of claim 8 above.

22. As per claim 20, Johnson has taught a method performing the same function as the processor of claim 9, consequently claim 20 is rejected for the same reasons set forth in the rejection of claim 9 above.

23. As per claim 23, Johnson discloses a system comprising:

A system memory including a plurality of addressable locations; (Fig. 6 memory 10)

And a microprocessor coupled to said system memory and comprising:

a plurality of functional units (Fig. 6 functional units 22-30), wherein said plurality of functional units is configured to collectively operate on a maximum number of operands in a given execution cycle; (Col. 4 lines 61-62)

a register file (Fig. 6 register file 18) providing a number of read ports that is insufficient to provide said maximum number of operands to said plurality of functional units in said given execution cycle; (Col. 4 lines 57-58)

and an arbitration logic (Fig. 9 decode arbitration 52) coupled to allocate said read ports of said register file for use by selected functional units during said given execution cycle. (Col. 4 lines 53-64)

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

25. Claims 5, 10 –11, 16, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson.

26. As per claim 5, Johnson discloses the microprocessor as recited in claim 3 wherein said first portion of said plurality of functional units includes an arithmetic logic unit (Fig. 6 ALU 24) configured to receive an operation during said given execution cycle. (Col. 3 line 63 - col. 4 line 2)

27. Johnson fails to disclose an address generation unit and wherein said arbitration logic is further configured to allocate said first portion of said read ports to said arithmetic logic unit in response to said arithmetic logic unit and said address generation unit each receiving an operation during said given execution cycle.

28. Fig. 6 discloses a plurality of ALUs (item 24). Using an ALU to calculate an effective address is extremely well-known in the art. A second ALU in Johnson's

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processor constitutes an address generation unit. Calculating an effective address with an ALU provides a destination address for use in changing program flow (ie, branching) and allows a program to perform conditional functions.

29. It would have been obvious to one of ordinary skill in the art at the time of invention to have used an ALU to calculate target addresses for the benefit of executing conditional branch statements.

30. The examiner asserts that any ports assigned to an instruction running on the primary ALU constitute the first portion of read ports, and those assigned to an instruction running on a second ALU (address generation unit) constitute the second group.

31. As per claim 10, Johnson discloses the microprocessor as recited in claim 1 further comprising a data forwarding unit (Fig. 6 result buffer 20) configured to store results produced by said plurality of functional units. *The examiner asserts that the bus entering result buffer 20 indicates that results from the functional units are stored therein.*

32. Johnson fails to disclose said arbitration logic is configured to allocate said results to said selected functional units during said given execution cycle prior to allocating said read ports of said register file.

33. Forwarding data from a result bus and using it in subsequent instructions is extremely well-known in the art. Using a result from an immediately prior operation by means of a forwarding unit allows computation of complex arithmetic/logical functions

without storing and retrieving the result from a register file, decreasing the demand for operand read ports.

34. It would have been obvious to one of ordinary skill in the art at the time of invention to have executed complex operations in multiple cycles by means of the result buffer, allocating the result to the subsequent instruction before allocating the register read ports for the benefit of reduced loads and stores in the register file, freeing up more read ports for other operands.

35. As per claim 11, Johnson discloses the microprocessor as recited in claim 1, but fails to disclose where said arbitration logic is further configured to allocate a single read port of said register file to one or more of said selected functional units.

36. Sharing a data source between multiple functional units is extremely well-known in the art. When a single read port provides operands for two instructions using a common input, another read port is freed for a third instruction to obtain an operand which provides for higher throughput and lower processing times.

37. It would have been obvious to one of ordinary skill in the art at the time of invention to have included logic to share each register file read port between multiple operand inputs of the functional units for the benefit of higher processor throughput.

38. As per claim 16, Johnson has taught a method performing the same function as the processor of claim 5, consequently claim 16 is rejected for the same reasons set forth in the rejection of claim 5 above.

39. As per claim 21, Johnson has taught a method performing the same function as the processor of claim 10, consequently claim 21 is rejected for the same reasons set forth in the rejection of claim 10 above.

40. As per claim 22, Johnson has taught a method performing the same function as the processor of claim 11, consequently claim 22 is rejected for the same reasons set forth in the rejection of claim 11 above.

Conclusion

41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Alidina et al. (U.S. Patent No. 6,175,912) disclose a processor with certain read ports of a register file assigned exclusively to certain functional units.

Van Eijndhoven et al. (U.S. Patent No. 6,076,154) disclose a multi-port register file and functional units capable of operating on more operands than the register file has read-ports.

Ando (U.S. Patent No. 5,918,065) discloses a system assigning a register file to multiple functional units.

42. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the

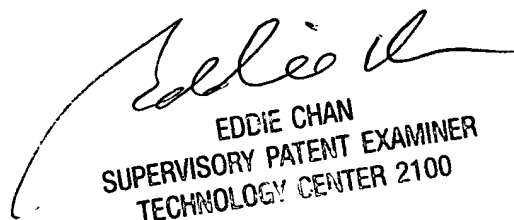
claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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